Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A memory device~~,~~ comprising:

a memory cell array having a multitude of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines, and one of said second wordlines;

each of said memory cells being accessible through one of said first wordlines and one of said first bitlines by an external port and being accessible through one of said second wordlines and one of said second bitlines by an internal port;

said external port being connected to input terminals to receive input signals in order to select one of said memory cells for an external data access; ~~and~~

a refresh control unit generating refresh control signals to control refreshing of the memory cells ~~access one of said memory cells to perform a refresh of the respective one of said memory cells~~ through said internal port; and

a contention detection circuit, said contention detection circuit receiving a row address in response to an external read or write access through said external port and receiving a refresh address for a row of memory cells to be refreshed, said contention detection circuit suppressing a refresh, if said refresh address equals said row address.

2. (currently amended) The memory device according to claim 1~~,~~ wherein each one of said memory cells comprises:

a first selection transistor coupled to one of said first wordlines and one of said first bitlines;

a second selection transistor coupled to one of said second wordlines and one of said second bitlines; and

a storage node connected to said first selection transistor and said second selection transistor.

3. (currently amended) The memory device according to claim 2, wherein each one of said memory cells comprises:

a storage transistor having a drain/source path and a gate terminal, said drain/source path being connected to said first and said second selection transistors; and

said gate terminal being connected to a reference potential.

4. (currently amended) The memory device according to claim 1, wherein said external port is connected to input terminals designed to receive one of an address signal, a signal determining a read or a write operation, a data clock signal, and a device select signal.

5. (currently amended) The memory device according to claim 4, wherein said internal port is hidden from said address signal, said signal determining a read or a write operation, and said device select signal.

6. (currently amended) The memory device according to claim 1, comprising:

a first bank of sense amplifiers, wherein each one of said first bitlines is connected to one of said sense amplifiers of said first bank; and

a column decoder, wherein an individual one of said sense amplifiers of said first bank can be selected to perform a memory access from ~~one of data read to~~ an external terminal. ~~; and data write from an external terminal.~~

7. (currently amended) The memory device according to claim 6~~,~~ comprising:

a second bank of sense amplifiers, wherein each one of said second bitlines is connected to one of said sense amplifiers of said second bank, and wherein multiple of said sense amplifiers are selected to perform a refresh of a row of memory cells.

8. (currently amended) The memory device according to claim 1~~,~~ comprising:

a first clock terminal to receive a system clock signal to synchronize external data input and output;

a second clock terminal to receive a reference clock signal; and

a synchronization circuit to output a refresh clock signal which is synchronized to one of said system clock or said reference clock signals.

9. (currently amended) The memory device according to claim 8~~,~~ comprising:

a refresh address counter to generate row addresses of rows of memory cells to be refreshed, said address counter being controlled by said refresh clock signal.

10. (currently amended) The memory device according to claim 8 ~~1, comprising:~~

~~a contention detection circuit, said contention detection circuit receiving a row address in response to an external read or write access through said external port and receiving a refresh address for a row of memory cells to be refreshed, said contention detection circuit suppressing a~~

~~refresh, if said refresh address equals said row address~~ wherein said memory cell array comprises at least two blocks of memory cells, said blocks being provided with a refresh row address in parallel, said refresh control unit generating a separate refresh enable signal for each of said blocks to perform a refresh operation for one of said blocks subsequent to a refresh operation for another one of said blocks.

11. (currently amended) The memory device according to claim 1, wherein said memory cell array comprises at least two blocks of memory cells, said blocks being provided with a refresh row address in parallel, said refresh control unit ~~circuit~~ generating a separate refresh enable signal for each of said blocks to perform a refresh operation for one of said blocks subsequent to a refresh operation for another one of said blocks.

12. (currently amended) A memory device, comprising:

a memory cell array having memory cells, each of said memory cells being accessible through a first port and through a second port, only said first port of said first and second ports being accessible by an external address signal to select one of said memory cells; and

a refresh control circuit designed to generate refresh control signals to refresh said memory cells through said second port; and

a contention detection circuit receiving a refresh address to access a subset of said memory cells and an address to access at least one of said memory cells of said subset of memory cells for an external read or write operation, said contention detection circuit suppressing a refresh operation for said subset of said memory cells.

13. (cancelled)

14. (currently amended) The memory device according to claim 12 ~~13,~~ wherein a refresh operation is performed for another subset of memory cells.

15. (currently amended) The memory device according to claim 12 ~~13,~~ wherein said subset of memory cells is a row of memory cells.

16. (currently amended) The memory device according to claim 12, wherein said refresh control circuit receives a system clock signal and a reference clock signal, said refresh control circuit has a refresh address counter to provide a sequence of addresses for subsets of memory cells to be refreshed, said memory device having a normal mode and a power-down mode, wherein said refresh address counter is controlled by said system clock signal during the normal mode and is controlled by said reference clock signal during the power-down mode.

17. (currently amended) The memory device according to claim 16, wherein said refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of said system clock or reference clock signals in response to one of said normal or power-down modes, wherein said clock signal controls said refresh address counter.

18. (currently amended) The memory device according to claim 16, wherein said reference clock signal has a lower frequency than said system clock signal.

19. (currently amended) The memory device according to claim 12, wherein each one of said memory cells comprises:

a first selection transistor coupled to the first port ~~one of said first wordlines and one of said first bitlines~~ and a second selection transistor coupled to the second port ~~one said second wordlines and one of said second bitlines~~; and

a storage node connected to said first selection transistor and said second selection transistor.

20. (currently amended) A memory device~~,~~ comprising:

a memory cell array having a multitude of memory cells arranged in rows;

a first row decoder to activate one of said rows in response to an external address;

a second row decoder to activate one of said rows in response to an internal address; and

a refresh control circuit to refresh the memory cells of a row which is activated by said second row decoder.

21. (currently amended) The memory device according to claim 20~~,~~ wherein said refresh control circuit comprises a contention detection circuit suppressing the refresh operation when the row to be activated by said first row decoder and the row to be activated by said second row decoder are the same row.

22. (currently amended) The memory device according to claim 20~~,~~ wherein each one of said memory cells comprises a first selection transistor connected to the first row decoder through a first wordline and a second selection transistor connected to the second row decoder through another wordline and a storage node coupled to the first and the second selection transistors.

23. (new) An integrated circuit (IC) comprising:

a multi-port memory cell array having at least first and second ports;

a plurality of memory cells accessible by the first and second ports

a refresh control unit generating refresh control signals to control refreshing of the memory cells through one of the ports; and

a contention detection circuit for detecting contention between refresh and memory access operations and suppressing refreshing operation when contention occurs.

24. (new) The IC of claim 23 wherein one of the ports comprises an internal access port for performing refreshing operations and the other one of the ports comprises an external port for performing memory access operations.

25. (new) The IC of claim 24 wherein:

the refresh control signals include a refresh address indicating location of a subgroup of memory cells of the array to be refreshed; and

the contention detection circuit suppressing refreshing operation when the memory access operation accesses a memory cell within the subgroup of memory cells to be refreshed.

26. (new) The IC of claim 25 wherein the subgroup of memory cells comprises at least one row of memory cells.

27. (new) The IC of claim 25 wherein the subgroup of memory cells comprises a row of memory cells.

28. (new) The IC of claim 23 wherein:

refresh control signals include a refresh address indicating location of a subgroup of memory cells of the array to be refreshed; and

the contention detection circuit suppressing refreshing operation when the memory access operation accesses a memory cell within the subgroup of memory cells to be refreshed.

29. (new) The IC of claim 28 wherein the subgroup of memory cells comprises at least one row of memory cells.

30. (new) The IC of claim 28 wherein the subgroup of memory cells comprises a row of memory cells.

31. (new) The IC of claim 23 wherein the refresh control circuit comprises a refresh address counter for generating refresh control signals corresponding to addresses of memory cells to be refreshed.

32. (new) The IC of claim 31 wherein a system clock signal and a reference clock signal are provided to the refresh control circuit, the system clock signal controls the refresh address counter when the memory array is operating in a normal mode of operation and the reference clock signal controls the refresh address counter when the memory array is in a power-down or reduced power mode of operation.

33. (new) The IC of claim 32 wherein the reference clock signal has a lower frequency than the system clock signal.

34. (new) The IC of claim 32 wherein the refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of the system or reference clock signals depending on the mode of operation of the memory array.

35. (new) The IC of claim 34 wherein the reference clock signal has a lower frequency than the system clock signal.